IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group art unit: 2841
Examiner: Yuriy Semenenko

In Re PATENT APPLICATION of:

Applicant(s): Seiichiro SASAKI et al.

Serial No.: 10/812,962

Filing Date: March 31, 2004

For: MULTILAYERED POWER SUPPLY LINE FOR SEMICONDUCTOR INTEGRATED CIRCUIT AND LAYOUT METHOD THEREOF

Atty. ref.: OKI 417

AMENDMENT

January 18, 2007

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is in response to the Official Action mailed on November 20, 2006. No extension-of-time fee is due. This paper is filed with an RCE, payment for which is attached. Please charge our Deposit Account No. 18-0002 if any additional fees are needed to enter this paper and/or the RCE paper, and please advise us accordingly. It is noted that no petition is required because of the authorization to charge, but this paper is a petition for extension of time if needed.